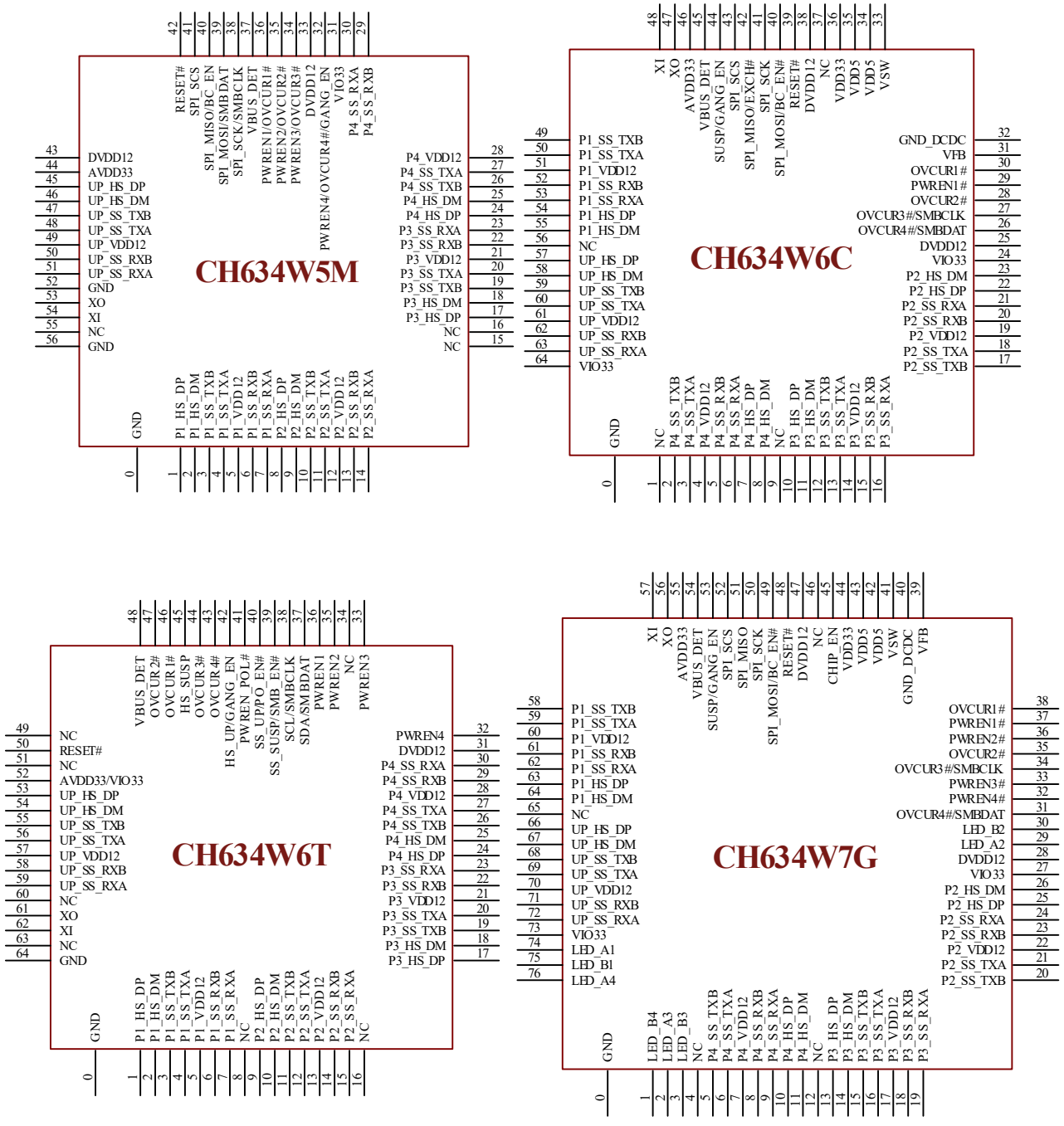
4-port USB3.0 HUB Controller Chip CH634

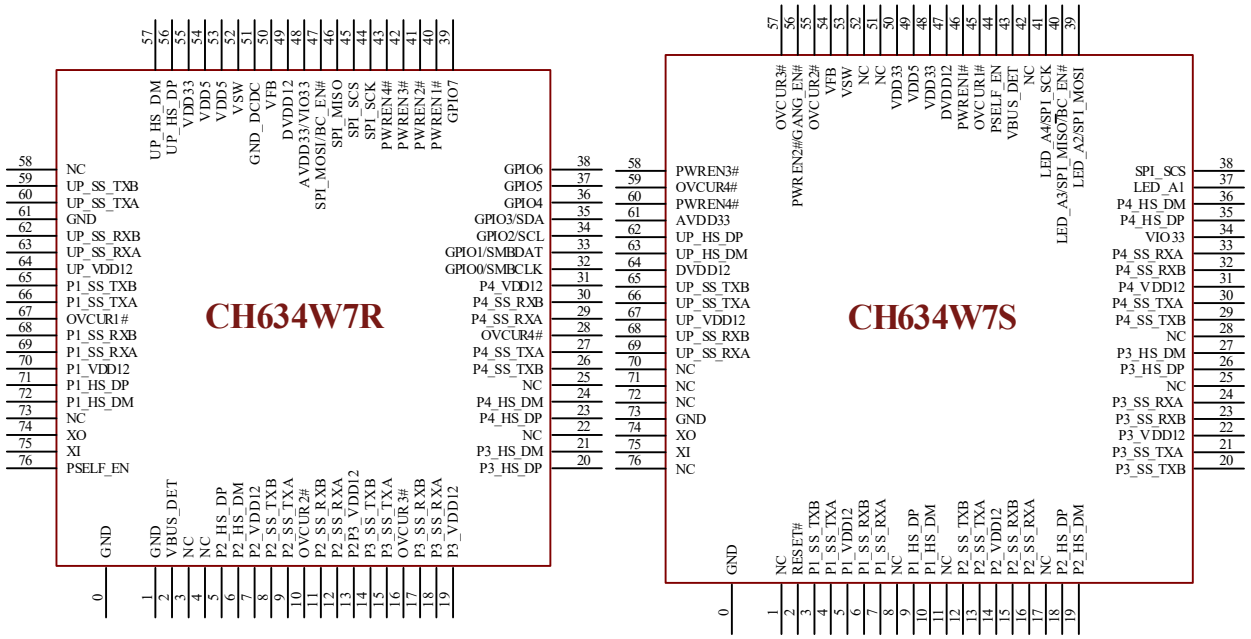
Datasheet 2

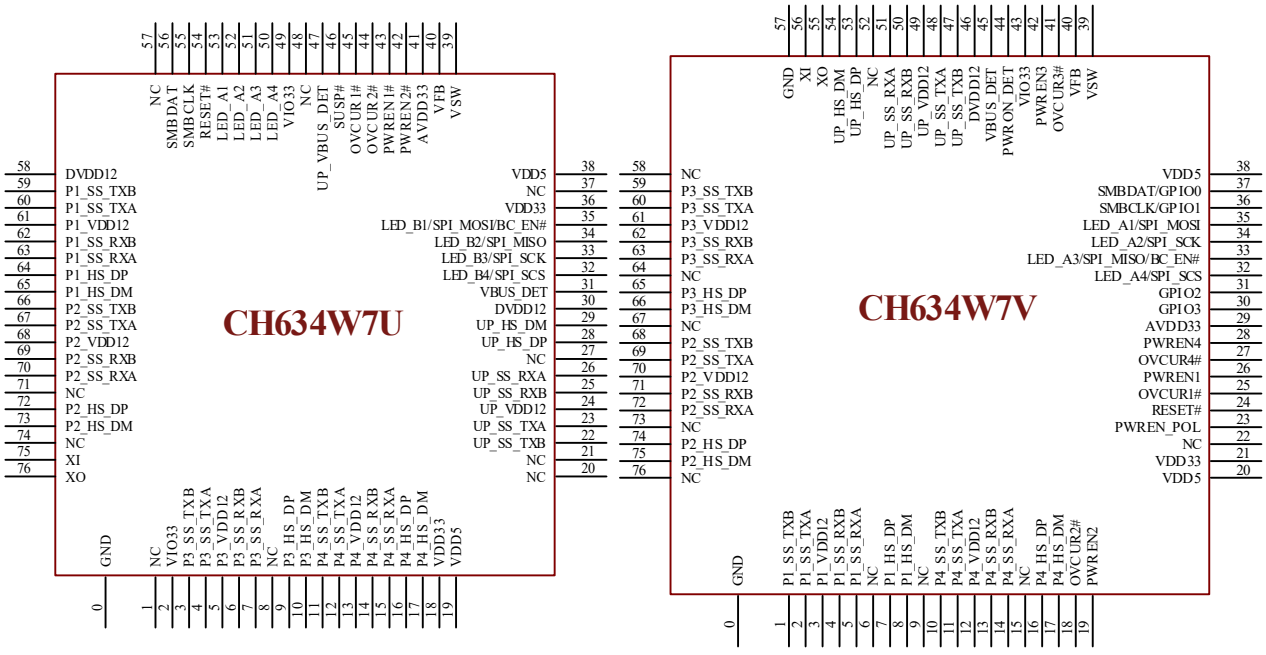
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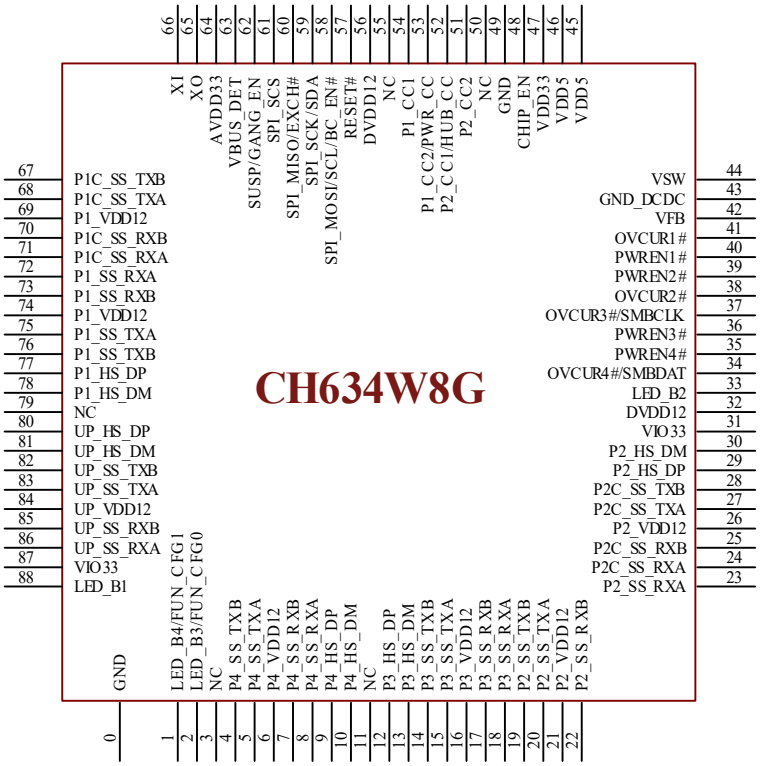
https://wch-ic.com

1. Pinouts




CH634W7R
CH634W7S


CH634W7U
CH634W7V



Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634F
QFN48	5*5mm	0.35mm	13.8mil	Quad Flat No-Lead Package	CH634M
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634X
QFN56	7*7mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W5M
QFN64	8*8mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W6C
QFN64	8*8mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W6G
QFN64X9	9*9mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH634W6T
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W7G
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W7R
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W7S
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W7U
QFN76	9*9mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W7V
QFN88	10*10mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W8G

Note: 1. Pin 0# is the EPAD of QFN package and is a necessary connection.

2. CH634F, CH634W5M and CH634W6T have no LDO voltage regulator and DC-DC step-down, and need external power supply of 3.3V and 1.2V at the same time. Other models have built-in 3.3V LDO voltage regulator and 1.2V DC-DC buck, and external single power supply is 5V or 3.3V.

3. The 4 downstream ports of CH634F include 2 USB3.2 Gen1 and 2 USB2.0; Other models include 4 USB3.2 Gen1 downstream ports and 4 USB2.0; Among them, CH634X and CH634W8G contain 2 sets of native Type-C/PD forward and backward insertion adaptive ports.

4. Custom pins CH634W5M, CH634W6C, CH634W6T, CH634W7G, CH634W7R, CH634W7S, CH634W7U, CH634W7V and CH634W8G are only reserved in lots.

5. For CH634F, CH634M, CH634X and CH634W6G, please refer to the CH634DS1 manual.

2. Pin Definitions

Table 2-1 USB signal related pin function description

USB signal pin	Pin name	Type(1)	Function description
Upstream port USBSS differential signal	UP_SS_TXA UP_SS_TXB	USB3	Upstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	UP_SS_RXA UP_SS_RXB	USB3	Upstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
Upstream port USB2.0 differential signal	UP_HS_DP	USB2	Upstream port USB2.0 differential signal D+。
	UP_HS_DM	USB2	Upstream port USB2.0 differential signal D-。
1#downstream port USBSS differential signal	P1_SS_TXA P1_SS_TXB	USB3	1#Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P1_SS_RXA P1_SS_RXB	USB3	1# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
1# downstream port USB2.0 differential signal	P1_HS_DP	USB2	1# Downstream port USB2.0 differential signal D+.
	P1_HS_DM	USB2	1# Downstream port USB2.0 differential signal D-。
2# downstream port USBSS differential signal	P2_SS_TXA P2_SS_TXB	USB3	2# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P2_SS_RXA P2_SS_RXB	USB3	2# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
2# downstream port USB2.0 differential signal	P2_HS_DP	USB2	2# Downstream port USB2.0 differential signal D+.
	P2_HS_DM	USB2	2# Downstream port USB2.0 differential signal D-.
3# downstream port USBSS differential signal	P3_SS_TXA P3_SS_TXB	USB3	3# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P3_SS_RXA P3_SS_RXB	USB3	3# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
3# downstream port USB2.0 differential signal	P3_HS_DP	USB2	3# Downstream port USB2.0 differential signal line D+。
	P3_HS_DM	USB2	3# Downstream port USB2.0 differential signal line D-。
4# downstream port USBSS differential signal	P4_SS_TXA P4_SS_TXB	USB3	4# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P4_SS_RXA P4_SS_RXB	USB3	4# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+(automatic cross identification).

4# downstream port USB2.0 differential signal	P4_HS_DP	USB2	4# Downstream port USB2.0 differential signal line D+.
	P4_HS_DM	USB2	4# Downstream port USB2.0 differential signal line D-.
1# or 2# downstream port Type-C differential signal	PxC_SS_TXA PxC_SS_TXB	USB3	1# or 2# Downstream port Type-C differential signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	PxC_SS_RXA PxC_SS_RXB	USB3	1# or 2# Downstream port Type-C differential signal line RX+/RX- or RX-/RX+ (automatic cross identification).

Table 2-2 CH634W5M pin definitions

Pin No.(See pin with the same name)	Pin name	Type(1)	Function description
44	AVDD33	P	3.3V analog power input; it is recommended to externally connect a 0.1uF capacitor in parallel with a 10uF decoupling capacitor.
43	DVDD12	P	1.2V core power input, it is recommended to connect an external 0.1uF capacitor in parallel with a 10uF decoupling capacitor.
33	DVDD12	P	1.2V core power input, it is recommended to connect an external 0.1uF capacitor in parallel with a 1uF decoupling capacitor.
31	VIO33	P	IO pin power supply input, external supply of 3.3V, it is recommended to externally connect 1uF or 0.1uF decoupling capacitor.
0	GND	P	Common ground terminal, GND must be connected.
52/56	GND	P	Optional ground terminal, GND connection recommended.
49	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor
5/28/21/12	Px_VDD12	P	1-4#downstream port 1.2V power input, external 0.1uF decoupling capacitor
54	XI	I	Crystal oscillator input terminal, connected to one end of an external 24MHz crystal and a capacitor to ground.
53	XO	O	The inverted output terminal of the crystal oscillator connects to the other end of an external 24MHz crystal and a capacitor to ground.
48/47/51/50	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
45/46	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
4/3/7/6	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
1/2	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line

11/10/14/13	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
8/9	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line
20/19/23/22	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
17/18	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line
27/26/30/29	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
24/25	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line
36	PWREN1	O	1#Downstream port power output control pin, high on.
	OVCUR1#	I	1#Downstream port overcurrent detection input pin, low overcurrent.
35	PWREN2	O	2#Downstream port power output control pin, high on.
	OVCUR2#	I	2#Downstream port overcurrent detection input pin, low overcurrent.
34	PWREN3	O	3#Downstream port power output control pin, high on.
	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
32	PWREN4	O	4#Downstream port power output control pin, high on.
	OVCUR4#	I	4#Downstream port overcurrent detection input pin, low overcurrent.
	GANG_EN	I	During reset, this pin functions as a configuration pin to set either integrated mode or independent mode. It incorporates an internal pull-down resistor. When left floating or connected to an external pull-down resistor, a low level indicates independent mode, while a high level indicates integrated mode.
37	VBUS_DET	I (FT)	USB bus VBUS status detection input. The VBUS power supply should be connected to this pin after being divided by two resistors. When this function is not used, this pin must be shorted to VIO33.
42	RESET#	I	External reset input with internal pull-up resistor. Active low. May be left floating when not in use. Recommended to short to AVDD33 for noise immunity.
41	SPI_SCS	O	SPI interface chip select output.
38	SPI_SCK	O	SPI interface clock output.
	SMBCLK	I	SMBus bus clock signal line.
39	SPI_MOSI	O	SPI interface data output.
	SMBDAT	I/O	SMBus bus data signal line
40	SPI_MISO	I	SPI interface data input, built-in pull-up resistors.
	BC_EN	I	During reset, this pin functions as a configuration pin to enable or disable the BC charging feature. It incorporates an internal pull-up resistor. Floating or a

			high logic level enables BC charging, while an external pull-down resistor set to a low logic level disables BC charging.
15/16/55	NC	-	Not connect, suggested suspension

Table 2-3 CH634W6C pin definitions

Pin No.(See pin with the same name)	Pin name	Type(1)	Function description
34	VDD5	P	DCDC power input, it is recommended to connect 10uF external capacitance to ground.
35			For the 5V power input of the 3.3V LDO, it is recommended to connect an external 1uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be shorted.
33	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
31	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
36	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
46	AVDD33	P	3.3V analog power input, it is recommended to connect 0.1uF parallel 10uF or 4.7uF decoupling capacitor.
38/25	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
24/64	VIO33	P	IO pin power supply input, external supply of 3.3V, it is recommended to externally connect 1uF or 0.1uF decoupling capacitor.
32	GND_DCDC	P	DCDC ground terminal, GND must be connected.
0	GND	P	Common ground terminal, GND must be connected.
61	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
51/19/14/4	Px_VDD12	P	1-4#Downstream port 1.2V power input, with an external 0.1uF decoupling capacitor.
48	XI	I	The input terminal of crystal oscillator is connected with one terminal of external 24MHz crystal and capacitor to ground.
47	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.

60/59/63/62	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
57/58	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
50/49/53/52	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
54/55	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
18/17/21/20	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
22/23	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
13/12/16/15	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
10/11	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
3/2/6/5	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
7/8	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
30	OVCUR1#	I	1#Downstream port overcurrent detection input pin, low overcurrent. In overall mode, downstream port overcurrent detection input pin, low level indicates overcurrent.
28	OVCUR2#	I	2#Downstream port overcurrent detection input pin, low overcurrent.
27	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
	SMBCLK		SMBus bus clock signal line.
26	OVCUR4#	I	4#Downstream port overcurrent detection input pin, low overcurrent.
	SMBDAT	I/O	SMBus bus data signal line.
29	PWREN1#	O	1#Downstream port power output control pin, low on. Overall mode downstream port power output control pin, low level enables.
39	RESET#	I	External reset input with internal pull-up resistor. Active low. May be left floating when not in use. Recommended to short to VDD33 to prevent interference.
40	SPI_MOSI	O	SPI interface data output.
	BC_EN#	I	During reset, this pin functions as a configuration pin to enable or disable the BC charging feature. It incorporates an internal pull-up resistor. Leaving it floating or setting it to a high-level disables BC charging. Adding an external pull-down resistor and setting it to a low level enables BC charging.
43	SPI_SCS	O	Chip select output for SPI interface.
41	SPI_SCK	O	Clock output for SPI interface.
42	SPI_MISO	I	SPI interface data input, built-in pull-up resistor.

	EXCH#		If the configuration parameter enables the upstream port switching function, the pin is switched to the uplink port and the 1#downlink port switching control input pin, suspended or pulled up without switching, and the input low level controls the switching.
45	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
44	SUSP	O	Sleep state output pin, which can be used to drive an LED. The output level during sleep is the same as the default state of the pull-up resistor configuration, and the output level during normal operation is opposite.
	GANG_EN	I	As a configuration pin during reset, it is used to configure global mode or independent mode. Built-in pull-up resistor, floating or high level is global mode, and external pull-down resistor is low level for independent mode.
1/9/37/56	NC	-	Not connect, suggested suspension

Table 2-4 CH634W6T pin definitions

Pin No. (See pin with the same name)	Pin name	Type(1)	Function description
52	AVDD33 /VIO33	P	3.3V analog power supply and I/O pin power input. It is recommended to externally connect a 0.1uF capacitor in parallel with a 10uF or 4.7uF decoupling capacitor.
31	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
0	GND	P	Common ground terminal, must be connected to GND.
64	GND	P	Optional ground terminal is recommended to be connected to GND.
57	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
5/28/21/13	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
62	XI	I	The input terminal of the crystal oscillator is connected to one end of an external 24MHz crystal and a capacitor to ground.
61	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.
56/55/59/58	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
53/54	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.

4/3/7/6	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
1/2	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
12/11/15/14	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
9/10	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
20/19/23/22	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
17/18	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
27/26/30/29	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
24/25	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
36	PWREN1	I/O	1#Downstream port power output control pin, high on. As a configuration pin during reset, it is used to configure whether the BC charging function is enabled on the 1#downstream port. The built-in pull-down resistor is set to low level to prohibit BC charging and high level to enable BC charging.
35	PWREN2	I/O	2#Downstream port power output control pin, high on. As a configuration pin during reset, it is used to configure whether the BC charging function is enabled on the 2#downstream port. The built-in pull-down resistor is set to low level to prohibit BC charging and high level to enable BC charging.
33	PWREN3	I/O	3#Downstream port power output control pin, high on. As a configuration pin during reset, it is used to configure whether the BC charging function is enabled on the 3#downstream port. The built-in pull-down resistor is set to low level to prohibit BC charging and high level to enable BC charging.
32	PWREN4	I/O	4#Downstream port power output control pin, high on. As a configuration pin during reset, it is used to configure whether the BC charging function is enabled on the 4#downstream port. The built-in pull-down resistor is set to low level to prohibit BC charging and high level to enable BC charging.
46	OVCUR1#	I	1#Downstream port overcurrent detection input pin, low overcurrent.
47	OVCUR2#	I	2#Downstream port overcurrent detection input pin, low overcurrent.
44	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
43	OVCUR4#	I (FT)	4#Downstream port overcurrent detection input pin, low overcurrent.

48	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
50	RESET#	I	External reset input, built-in pull-up resistor, active low level, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
39	SS_SUSP	O	SuperSpeed USB interface sleep state output pin, high level indicates sleep state, low level indicates normal state.
	SMB_EN#	I	Used as a configuration pin during reset to select I2C and SMBus interfaces, built-in pull-up resistor, floating or high to select I2C interface, and additional pull-down resistor to set low to select SMBus interface.
45	HS_SUSP	O	Sleep state output pin of high-speed USB interface, high level indicates sleep state, low level indicates normal state.
40	SS_UP	O	Upstream SuperSpeed USB interface connection status output pin, high indicates connected, low indicates not connected.
	PO_EN#	I (FT)	During reset, it is used as configuration pin to configure whether to enable power control and overcurrent function. Built-in pull-down resistor is set to low level by floating or external pull-down resistor to enable power control and overcurrent function, otherwise power control and overcurrent function are disabled.
42	HS_UP	O	Upstream high-speed USB interface connection status output pin, high indicates connected, low indicates not connected.
	GANG_EN	I (FT)	As a configuration pin during reset, it is used to configure global mode or independent mode. Built-in pull-up resistor, floating or high level is global mode, and external pull-down resistor is low level for independent mode.
41	PWREN_POL#	I (FT)	As a configuration pin during reset, it is used to configure the output polarity of the power control pin. Built-in pull-up resistor is used to set the output high level to be active when floating or high level, and the external pull-down resistor is used to set the output low level to be active low level.
38	SCL	O	Clock signal line for 2-wire serial interface.

	SMBCLK	I	SMBus bus clock signal line.
37	SDA	I/O	Data signal line for 2-wire serial interface.
	SMBDAT	I/O	SMBus bus data signal line.
8/16/34/49/51/60/63	NC	-	Not connect, suggested suspension

Table 2-5 CH634W7G pin definitions

Pin No. (See pin with the same name)	Pin name	Type(1)	Function description
42	VDD5	P	DCDC power input, it is recommended to connect 10uF external capacitance to ground.
43	VDD5	P	For the 5V power input of the 3.3V LDO, it is recommended to connect an external 1uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be shorted.
41	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
39	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
44	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
55	AVDD33	P	3.3V analog power input, it is recommended to connect 0.1uF parallel 10uF or 4.7uF decoupling capacitor.
28/47	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
27/73	VIO33	P	IO pin power supply input, external supply of 3.3V, it is recommended to externally connect 1uF or 0.1uF decoupling capacitor.
40	GND_DCDC	P	DCDC ground terminal, GND must be connected.
0	GND	P	Common ground terminal, GND must be connected.
70	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
60/22/17/7	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
57	XI	I	The input terminal of the crystal oscillator is connected to one end of an external 24MHz crystal and a capacitor to ground.
56	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.

69/68/72/71	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
66/67	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
59/58/62/61	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
63/64	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
21/20/24/23	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
25/26	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
16/15/19/18	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
13/14	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
6/5/9/8	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
10/11	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
37	PWREN1#	O	1#Downstream port power output control pin, low on.
36	PWREN2#	O	2# Downstream port power output control pin, low on.
33	PWREN3#	O	3# Downstream port power output control pin, low on.
32	PWREN4#	O	4# Downstream port power output control pin, low on.
38	OVCUR1#	I	1# Downstream port overcurrent detection input pin, low overcurrent.
35	OVCUR2#	I	2# Downstream port overcurrent detection input pin, low overcurrent.
34	OVCUR3#/	I	3# Downstream port overcurrent detection input pin, low overcurrent.
	SMBCLK		SMBus bus clock signal line.
31	OVCUR4#/	I	4# Downstream port overcurrent detection input pin, low overcurrent.
	SMBDAT	I/O	SMBus bus data signal line.
54	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
48	RESET#	I	External reset input, built-in pull-up resistor, active low level, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
53	SUSP	O	Sleep state output pin, which can be used to drive an LED. The output level during sleep is the same as the default state of the pull-up resistor configuration, and the output level during normal operation is opposite.
	GANG_EN	I	As a configuration pin during reset, it is used to configure global mode or independent mode. Built-in pull-up resistor, floating or high level is global mode,

			and external pull-down resistor is low level for independent mode.
45	CHIP_EN	I (FT)	Chip enable control, low level control chip into low power consumption mode, high level control chip into normal operation mode.
52	SPI_SCS	O	Chip select output for SPI interface.
50	SPI_SCK	O	Clock output for SPI interface.
49	SPI_MOSI	O	Data output for SPI interface.
	BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
51	SPI_MISO	I	SPI interface data input, built-in pull-up resistor.
74	LED_A1	O	1#Downstream port normal status indication signal.
29	LED_A2	O	2#Downstream port normal status indication signal.
2	LED_A3	O	3#Downstream port normal status indication signal.
76	LED_A4	O	4#Downstream port normal status indication signal.
75	LED_B1	O	1#Downstream port abnormal status indication signal.
30	LED_B2	O	2#Downstream port abnormal status indication signal.
3	LED_B3	O	3#Downstream port abnormal status indication signal.
1	LED_B4	O	4#Downstream port abnormal status indication signal.
4/12/46/65	NC	-	Not connect, suggested suspension

Table 2-6 CH634W7R pin definitions

Pin No. (See pin with the same name)	Pin name	Type(1)	Function description
53	VDD5	P	DCDC power input, it is recommended to connect 10uF external capacitance to ground.
54	VDD5	P	For the 5V power input of the 3.3V LDO, it is recommended to connect an external 1uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be shorted.
52	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
50	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
55	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
48	AVDD33	P	3.3V analog power input, it is recommended to connect

	/VIO33		0.1uF parallel 10uF or 4.7uF decoupling capacitor.
49	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
51	GND_DCDC	P	DCDC ground terminal, GND must be connected.
0/61	GND	P	Common ground terminal, GND must be connected.
1	GND	P	Optional ground terminal, GND must be connected.
64	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
70/7/13/19/31	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
75	XI	I	The input terminal of the crystal oscillator is connected to one end of an external 24MHz crystal and a capacitor to ground.
74	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.
60/59/63/62	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
56/57	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
66/65/69/68	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
71/72	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
9/8/12/11	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
5/6	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
15/14/18/17	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
20/21	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
27/26/29/30	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
23/24	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
40	PWREN1#	O	1#Downstream port power output control pin, low on.
41	PWREN2#	O	2# Downstream port power output control pin, low on.
42	PWREN3#	O	3# Downstream port power output control pin, low on.
43	PWREN4#	O	4# Downstream port power output control pin, low on.
67	OVCUR1#	I (FT)	1#Downstream port overcurrent detection input pin, low overcurrent.
10	OVCUR2#	I (FT)	2#Downstream port overcurrent detection input pin, low overcurrent.
16	OVCUR3#	I (FT)	3#Downstream port overcurrent detection input pin, low overcurrent.
28	OVCUR4#	I (FT)	4#Downstream port overcurrent detection input pin, low overcurrent.
2	VBUS_DET	I	USB bus VBUS status detection input, VBUS power

		(FT)	should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
76	PSELF_EN	I	Used as a configuration pin during reset to configure power supply mode, built-in pull-up resistor, floating or high level for self-power supply mode, external pull-down resistor set low level for bus power supply mode.
45	SPI_SCS	O	Chip select output for SPI interface.
44	SPI_SCK	O	Clock output for SPI interface.
47	SPI_MOSI	O	Data output for SPI interface.
	BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
46	SPI_MISO	I	SPI interface data input, built-in pull-up resistor.
32	GPIO0	I/O (FT)	General-purpose GPIO0, used for input or output on the I/O port. Factory default: Indicates normal status on #1 downstream.
	SMBCLK	I	SMBus bus clock signal line.
33	GPIO1	I/O	General-purpose GPIO1, used for input or output. Factory default: Indicates abnormal status on #1 downstream.
	SMBDAT	I/O	SMBus bus data signal line.
34	GPIO2	I/O	General-purpose GPIO2, used for input or output. Factory default: Indicates normal status on #2 downstream.
	SCL	O	Clock signal line of 2-wire serial interface
35	GPIO3	I/O	General-purpose GPIO3, used for input or output. Factory default: Indicates abnormal status on #2 downstream.
	SDA	I/O	Data signal line of 2-wire serial interface
36	GPIO4	I/O	General-purpose GPIO4, used for input or output. Factory default: Indicates normal status on #3 downstream.
37	GPIO5	I/O	General-purpose GPIO5, used for input or output. Factory default: Indicates abnormal status on #3 downstream.
38	GPIO6	I/O	General-purpose GPIO6, used for input or output. Factory default: Indicates normal status on #4 downstream.
39	GPIO7	I/O	General-purpose GPIO7, used for input or output.

			Factory default: Indicates abnormal status on #4 downstream. It is used as a configuration pin during reset to configure whether to enable the SMbus function. It has a built-in pull-up resistor. If left floating or high, it enables the I2C function and disables the SMbus function. An additional pull-down resistor, set low, enables the SMbus function and disables the I2C function.
3/4/22/25/58/73	NC	-	Not connect, suggested suspension.

Table 2-7 CH634W7S pin definitions

Pin No. (See pin with the same name)	Pin name	Type(1)	Function description
49	VDD5	P	5V power input; it is recommended to connect an external 1uF capacitor in parallel with a 10uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be shorted.
53	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
54	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
48	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
50	VDD33	P	3.3V auxiliary power terminal, connect to other VDD33 sources. It is recommended to add an external 1uF decoupling capacitor.
61	AVDD33	P	3.3V analog power input; it is recommended to externally connect a 0.1uF capacitor in parallel with a 10uF or 4.7uF decoupling capacitor.
34	VIO33	P	IO pin power input, externally supplied with 3.3V. It is recommended to connect an external 1uF or 0.1uF decoupling capacitor.
47/64	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
0	GND	P	Common ground terminal, GND must be connected.
73	GND	P	Optional ground terminal, GND must be connected.
67	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
5/14/22/31	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
75	XI	I	The input terminal of the crystal oscillator is connected to

<table>
<tr><td></td><td></td><td></td><td>one end of an external 24MHz crystal and a capacitor to ground.</td></tr>
<tr><td>74</td><td>XO</td><td>O</td><td>The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.</td></tr>
<tr><td>66/65/69/68</td><td>UP_SS_xxx</td><td>USB3</td><td>Upstream port USBSS differential transmit or receive signal line.</td></tr>
<tr><td>62/63</td><td>UP_HS_xx</td><td>USB2</td><td>Upstream port USB2.0 differential signal line.</td></tr>
<tr><td>4/3/7/6</td><td>P1_SS_xxx</td><td>USB3</td><td>1#Downstream port USBSS differential transmit or receive signal line.</td></tr>
<tr><td>9/10</td><td>P1_HS_xx</td><td>USB2</td><td>1#Downstream port USB2.0 differential signal line.</td></tr>
<tr><td>13/12/16/15</td><td>P2_SS_xxx</td><td>USB3</td><td>2#Downstream port USBSS differential transmit or receive signal line.</td></tr>
<tr><td>18/19</td><td>P2_HS_xx</td><td>USB2</td><td>2#Downstream port USB2.0 differential signal line.</td></tr>
<tr><td>21/20/24/23</td><td>P3_SS_xxx</td><td>USB3</td><td>3#Downstream port USBSS differential transmit or receive signal line.</td></tr>
<tr><td>26/27</td><td>P3_HS_xx</td><td>USB2</td><td>3#Downstream port USB2.0 differential signal line.</td></tr>
<tr><td>30/29/33/32</td><td>P4_SS_xxx</td><td>USB3</td><td>4#Downstream port USBSS differential transmit or receive signal line.</td></tr>
<tr><td>35/36</td><td>P4_HS_xx</td><td>USB2</td><td>4#Downstream port USB2.0 differential signal line.</td></tr>
<tr><td>46</td><td>PWREN1#</td><td>O</td><td>1#Downstream port power output control pin, low on.</td></tr>
<tr><td rowspan="2">56</td><td>PWREN2#</td><td>O</td><td>2#Downstream port power output control pin, low on.</td></tr>
<tr><td>GANG_EN#</td><td>I</td><td>As a configuration pin during reset, it is used to configure global mode or independent mode. Built-in pull-up resistor, floating or high level is global mode, and external pull-down resistor is low level for independent mode.</td></tr>
<tr><td rowspan="2">58</td><td rowspan="2">PWREN3#</td><td>O</td><td>3#Downstream port power output control pin, low on.</td></tr>
<tr><td>I</td><td>Configure pin 0 as the number of downstream ports during reset, in conjunction with the PWREN4# pin.</td></tr>
<tr><td rowspan="2">60</td><td rowspan="2">PWREN4#</td><td>O</td><td>4#Downstream port power output control pin, low on.</td></tr>
<tr><td>I</td><td>Configure pin 0 as the number of downstream ports during reset, in conjunction with the PWREN3# pin.
<table>
<tr><th>PWREN4# Level</th><th>PWREN3# Level</th><th>Downstream ports number</th></tr>
<tr><td>0</td><td>0</td><td>2 (3# and 4#disabled)</td></tr>
<tr><td>0</td><td>1</td><td>3 (4# disabled)</td></tr>
<tr><td>1</td><td>0</td><td>Invalid configuration</td></tr>
<tr><td>1</td><td>1</td><td>4</td></tr>
</table></td></tr>
<tr><td>45</td><td>OVCUR1#</td><td>I</td><td>1#Downstream port overcurrent detection input pin, low</td></tr>
</table>

			overcurrent.
55	OVCUR2#	I (FT)	2#Downstream port overcurrent detection input pin, low overcurrent.
57	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
59	OVCUR4#	I	4#Downstream port overcurrent detection input pin, low overcurrent.
43	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
44	PSELF_EN	I	Used as a configuration pin during reset to configure power supply mode, built-in pull-up resistor, floating or high level for self-power supply mode, external pull-down resistor set low level for bus power supply mode.
38	SPI_SCS	O	Chip select output for SPI interface.
41	LED_A4	O	4#Downstream port normal status indication signal.
	SPI_SCK		Clock output for SPI interface.
40	LED_A3	O	3#Downstream port normal status indication signal.
	SPI_MOSI	0	The data input of the SPI interface has a built-in pull-up resistor.
	BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
39	LED_A2	O	2#Downstream port normal status indication signal.
	SPI_MOSI	I	Data output of SPI interface.
37	LED_A1	I/O	1#Downstream port normal status indication signal.
2	RESET#	I	External reset input, built-in pull-up resistor, active low level, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
1/8/11/17/25/28/42/51/52/70/71/72/76	NC	-	Not connect, suggested suspension.

Table 2-8 CH634W7U and CH634W7V pin definitions

Pin No. (See pin with the same name)		Pin name	Type(1)	Function description
CH634W7U	CH634W7V			
38	38	VDD5	P	DCDC power input, it is recommended to connect 10uF external capacitance to ground.
19	20	VDD5	P	For the 5V power input of the 3.3V LDO, it is recommended to connect an external 1uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be

				shorted.
39	39	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
40	40	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
36	21	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
18	-	VDD33	P	3.3V auxiliary power terminal, connect to other VDD33 sources. It is recommended to add an external 1uF decoupling capacitor.
41	29	AVDD33	P	3.3V analog power input; it is recommended to externally connect a 0.1uF capacitor in parallel with a 10uF or 4.7uF decoupling capacitor.
30/58	46	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
2/49	43	VIO33	P	IO pin power input, externally supplied with 3.3V. It is recommended to connect an external 1uF or 0.1uF decoupling capacitor.
0	0	GND	P	Common ground terminal, GND must be connected.
-	57	GND	P	Optional ground terminal, GND must be connected.
24	49	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
61/68/5/13	3/70/61/12	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
75	56	XI	I	The input terminal of the crystal oscillator is connected to one end of an external 24MHz crystal and a capacitor to ground.
76	55	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.
23/22/26/25	48/47/51/50	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
28/29	53/54	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
60/59/63/62	2/1/5/4	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
64/65	7/8	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
67/66/70/69	69/68/72/71	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
72/73	74/75	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
4/3/7/6	60/59/63/62	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or

				receive signal line.
9/10	65/66	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
12/11/15/14	11/10/14/13	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
16/17	16/17	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
45	25	OVCUR1#	I	1#Downstream port overcurrent detection input pin, low overcurrent. Overall mode downstream port overcurrent detection input pin, low on.
44	18	OVCUR2#	I	2#Downstream port overcurrent detection input pin, low overcurrent.
-	41	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
-	27	OVCUR4#	I	4#Downstream port overcurrent detection input pin, low overcurrent.
43	-	PWREN1#	O	1#Downstream port power output control pin, low on.
42	-	PWREN2#	O	2#Downstream port power output control pin, low on.
-	26	PWREN1	O	1#Downstream port power output control pin, high on. Overall mode downstream port power output control pin, high on.
-	19	PWREN2	O	2#Downstream port power output control pin, high on.
-	42	PWREN3	O	3#Downstream port power output control pin, high on.
-	28	PWREN4	O	4#Downstream port power output control pin, high on.
54	24	RESET#	I	External reset input, built-in pull-up resistor, active low, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
-	32	LED_A4	O	4#Downstream port normal status indication signal.
		SPI_SCS	O	Chip select output for SPI interface.
-	34	LED_A2	O	2#Downstream port normal status indication signal.
		SPI_SCK	O	Clock output for SPI interface.
-	33	LED_A3	O	3#Downstream port normal status indication signal.
		SPI_MISO	I	The data input of the SPI interface has a built-in pull-up resistor.
		BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
-	35	LED_A1	O	1#Downstream port normal status indication signal.
		SPI_MOSI	I	The data output of the SPI interface
32	-	LED_B4	O	4#Downstream port abnormal status indication signal.
		SPI_SCS		Chip select output for SPI interface.
33	-	LED_B3	O	3#Downstream port abnormal status indication signal.
		SPI_SCK		Clock output for SPI interface.

35	-	LED_B1	O	1#Downstream port abnormal status indication signal.
		SPI_MOSI	O	Data output for SPI interface.
		BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
34	-	LED_B2	O	2#Downstream port abnormal status indication signal.
		SPI_MISO	I	SPI interface data input, built-in pull-up resistor.
53	-	LED_A1	O	1#Downstream port normal status indication signal.
52	-	LED_A2	O	2#Downstream port normal status indication signal.
51	-	LED_A3	O	3#Downstream port normal status indication signal.
50	-	LED_A4	O	4#Downstream port normal status indication signal.
31	45	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
46	-	SUSP#	O	SUSP sleep state output pin, high level indicates sleep state, low level indicates normal state.
47	-	UP_VBUS_DET	I (FT)	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
-	44	PWRON_DET	I	External power status detection input, built-in pull-down resistor, high level means external power connection is detected, low level means external power connection is not detected.
-	23	PWREN_POL	I	As a configuration pin during reset, it is used to configure the output polarity of the power control pin. Floating or high level is active low level of the output, and the external pull-down resistor sets low level to active high level of the output.
55	36	SMBCLK	I	SMBus bus clock signal line.
		GPIO1	I/O	General-purpose GPIO1, used for input or output.
56	37	SMBDAT	I/O	SMBus bus data signal line.
		GPIO0	I/O	General-purpose GPIO0, used for input or output.
-	31	GPIO2	I/O	General-purpose GPIO2, used for input or output.
-	30	GPIO3	I/O	General-purpose GPIO3, used for input or output.
1/8/20/21/27/37/41/48/57/71/74	6/9/15/22/52/58/64/67/73/76	NC	-	Not connect, suggested suspension.

Table 2-9 CH634W8G pin definitions

Pin No. (See pin with the same name)	Pin name	Type(1)	Function description

45	VDD5	P	DCDC power input, it is recommended to connect 10uF external capacitance to ground.
46	VDD5	P	For the 5V power input of the 3.3V LDO, it is recommended to connect an external 1uF capacitor. If the VDD5 voltage is less than 3.6V, VDD33 should be shorted.
44	VSW	P	DCDC output terminal, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed nearby to the ground capacitor, it is recommended to use 2.2uH inductor and at least one 10uF capacitor.
42	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
47	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
64	AVDD33	P	3.3V analog power input, it is recommended to connect 0.1uF parallel 10uF or 4.7uF decoupling capacitor.
31/87	VIO33	P	IO pin power input, externally supplied with 3.3V. It is recommended to connect an external 1uF or 0.1uF decoupling capacitor.
32/56	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
43	GND_DCDC	P	DCDC ground terminal, GND must be connected.
0	GND	P	Common ground terminal, GND must be connected.
49	GND	P	Optional ground terminal, GND must be connected.
84	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
69(74)/21(26)/16/6	Px_VDD12	P	1-4#Downstream port 1.2V power input, external 0.1uF decoupling capacitor.
66	XI	I	The input terminal of the crystal oscillator is connected to one end of an external 24MHz crystal and a capacitor to ground.
65	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.
83/82/86/85	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
80/81	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
75/76/72/73	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
68/67/71/70	P1C_SS_xxx	USB3	1#Downstream port Type-C differential transmit or receive signal line.
77/78	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.

20/19/23/22	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
27/28/24/25	P2C_SS_xxx	USB3	2#Downstream port Type-C differential transmit or receive signal line.
29/30	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
15/14/18/17	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
12/13	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
5/4/8/7	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
9/10	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
40	PWREN1#	O	1#Downstream port power output control pin, low on.
39	PWREN2#	O	2# Downstream port power output control pin, low on.
36	PWREN3#	O	3# Downstream port power output control pin, low on.
35	PWREN4#	O	4# Downstream port power output control pin, low on.
41	OVCUR1#	I	1#Downstream port overcurrent detection input pin, low overcurrent.
38	OVCUR2#	I	2#Downstream port overcurrent detection input pin, low overcurrent.
37	OVCUR3#	I	3#Downstream port overcurrent detection input pin, low overcurrent.
	SMBCLK		SMBus bus clock signal line.
34	OVCUR4#	I	4#Downstream port overcurrent detection input pin, low overcurrent.
	SMBDAT	I/O	SMBus bus data signal line.
63	VBUS_DET	I	USB bus VBUS status detection input, VBUS power should be connected to this pin after voltage division through two resistors; when this function is not used, this pin needs to be shorted to VIO33.。
62	SUSP	0	Sleep state output pin, which can be used to drive LED. The output level is the same as the default state of the pull-up and pull-down resistor configuration during sleep, but the output level is opposite during normal operation.
	GANG_EN	I	As a configuration pin during reset, it is used to configure global mode or independent mode. Built-in pull-up resistor, floating or high level is global mode, and external pull-down resistor is low level for independent mode.
48	CHIP_EN	I	Chip enable control; Low level controls the chip to enter low-power mode, while high level controls the chip to enter normal operating mode.
61	SPI_SCS	O	Chip select output for SPI interface.

59	SPI_SCK	O	Clock select output for SPI interface.
	SDA	I/O	PD-HUB Mode: The data signal line of the 2-wire serial interface, used to connect the CH211 chip.
58	SPI_MOSI	O	Data output for SPI interface.
	SCL	I/O	PD-HUB Mode: The clock signal line of the 2-wire serial interface, used to connect the CH211 chip.
	BC_EN#	I	As a configuration pin during reset, it is used to configure whether to enable BC charging function. Built-in pull-up resistor, floating or high level prohibits BC charging, and external pull-down resistor sets low level to enable BC charging.
60	SPI_MISO	I	SPI interface data input, built-in pull-up resistor.
	EXCH#		If the configuration parameter enables the upstream port switching function, the pin is switched to the upstream port and the 1#downstream port switching control input pin, suspended or pulled up without switching, and the input low level controls the switching.
57	RESET#	I	External reset input, built-in pull-up resistor, active low level, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
88	LED_B1	O	1#Downstream port abnormal status indication signal.
33	LED_B2	O	2#Downstream port abnormal status indication signal.
2	LED_B3	O	3#Downstream port abnormal status indication signal.
	FUN_CFG0	I	Pin 0 is configured as the C port operating mode during reset and is functionally configured with the FUN_CFG1 pin, see Table 5-5.
1	LED_B4	O	4# Downstream port abnormal status indication signal.
	FUN_CFG1	I	Pin 1 is configured as the C port operating mode during reset and is functionally configured with the FUN_CFG1 pin, see Table 5-5.
54	P1_CC1	I/O (FT)	General HUB mode: 1# downstream port PD protocol communication pin CC1. PD-HUB mode: 1# downstream port PD protocol communication pin CC1. In general HUB mode with SMBus off, if EXCH# is low, the pin switches to the PD protocol communication pin CC1 of the new upstream port as the downstream port of 1. If switched to the upstream port, this pin needs to be grounded via a 5.1K resistor. If P1_CC1 is grounded through a 5.1K resistor, the P1C_SS* signal is invalid and port 1# is changed from port C to port A.
53	P1_CC2	I/O (FT)	General HUB mode: 1# downstream port PD protocol communication pin CC2. In general HUB mode with

			SMBus off, if EXCH# is low, the pin switches to the PD protocol communication pin CC2 of the new upstream port as the downstream port of 1. If switched to the upstream port, this pin needs to be grounded via a 5.1K resistor. If P1_CC2 is grounded through a 5.1K resistor, the P1_SS* signal is invalid and port 1# is changed from port C to port A, and P1_SS* signal pin is optionally used.
	PWR_CC	I/O	PD-HUB mode: the external power supply terminal PD protocol communication pin is used to connect the Type-C power adapter.
52	P2_CC1	I/O (FT)	General HUB mode: 2# downstream port PD protocol communication pin CC1. If P2_CC1 is grounded through a 5.1K resistor, the P2C_SS* signal is invalid, and the 2# port is changed from port C to port A..
	HUB_CC	I/O	PD-HUB mode: the communication pin of upstream PD protocol is used to connect USB hosts such as mobile phones/computers.
51	P2_CC2	I/O (FT)	General HUB mode: 2# downstream port PD protocol communication pin CC2. If P2_CC2 is grounded through a 5.1K resistor, the P2_SS* signal is invalid, the 2# port is changed from port C to port A, and the P2C_SS* signal pin is selected. PD-HUB mode: 1# downstream port PD protocol communication pin CC2.
3/11/50/55/79	NC	-	Not connect, suggested suspension.

Note 1: Pin type abbreviation explanation:

USB3 = USB3.0 signal pin;

USB2 = USB2.0 signal pin;

I = Signal input;

O = Signal output;

P = Power or ground;

NC = Reserved;

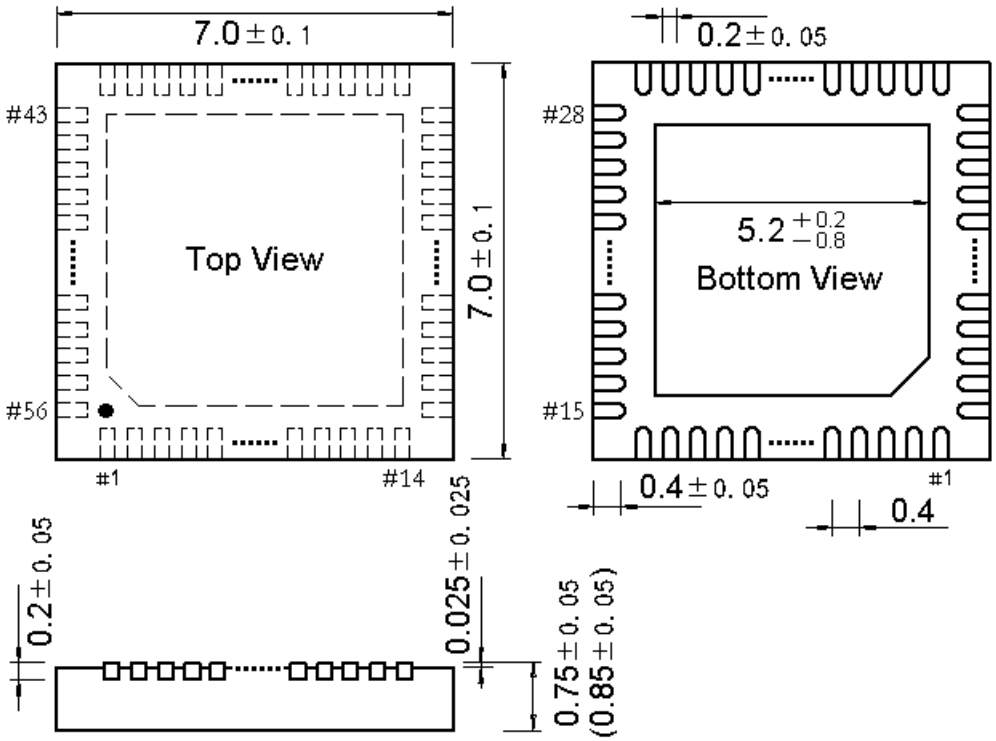
FT = Tolerant 5V voltage.

3. Package Information

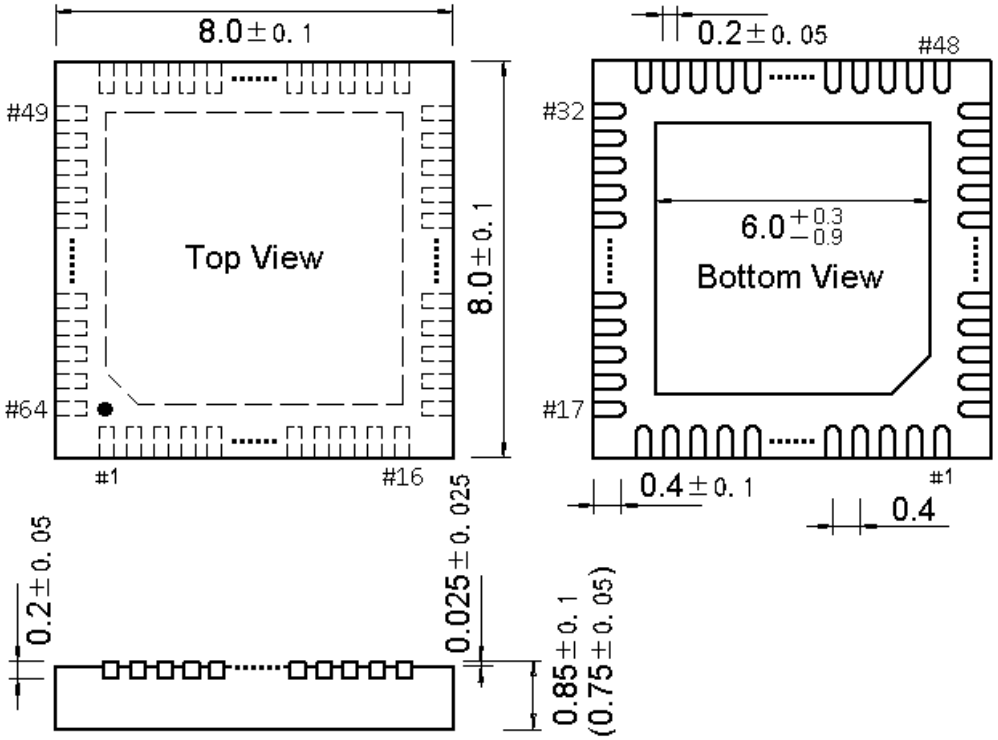
Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

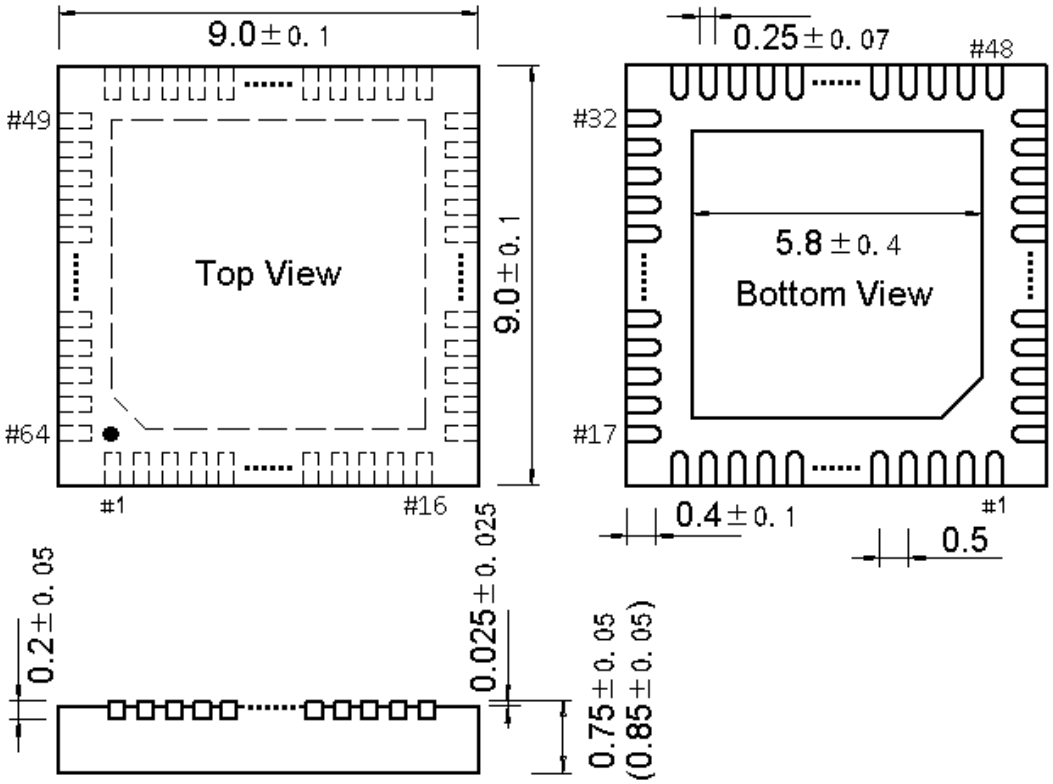
3.1 QFN56



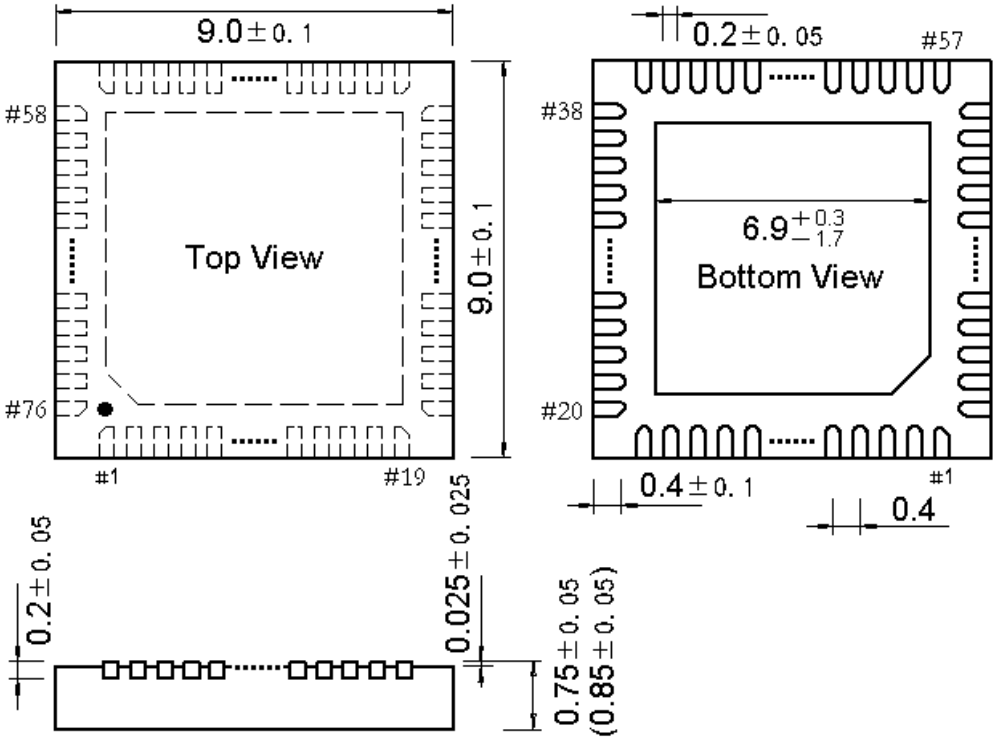
3.2 QFN64


8.0±0.1
#49
#64
#1
#16
Top View
8.0±0.1
0.2±0.05
#48
#32
#17
#1
6.0 +0.3 −0.9
Bottom View
0.4±0.1
0.4
0.2±0.05
0.025±0.025
0.85±0.1
(0.75±0.05)

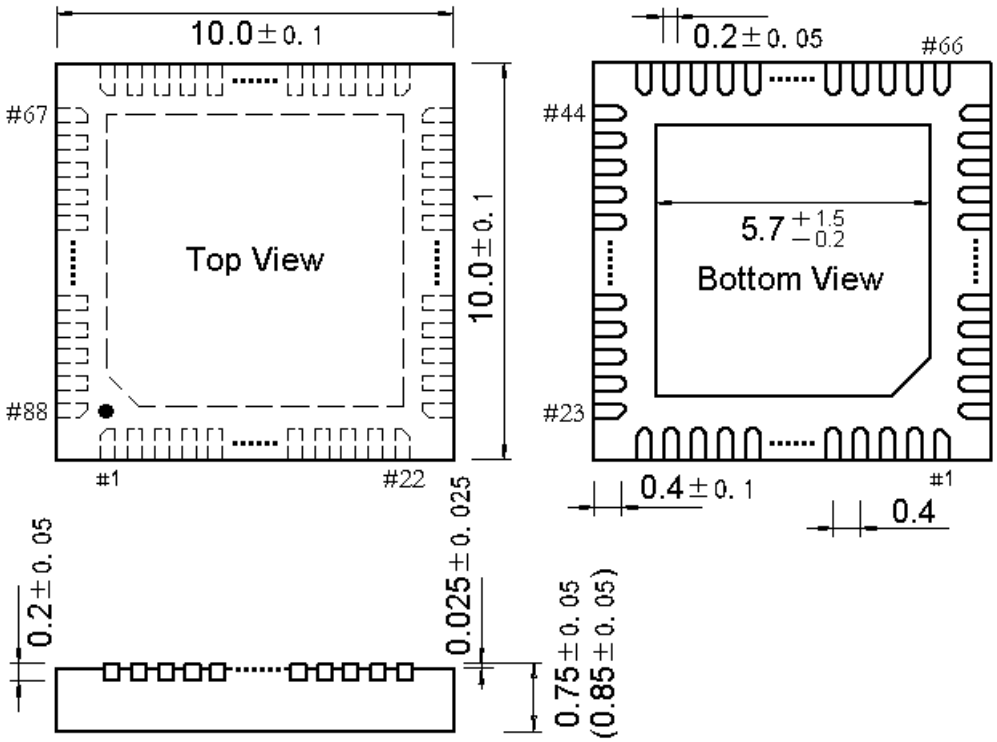
3.3 QFN64X9


9.0±0.1
#49
#64
#1
#16
Top View
9.0±0.1
0.25±0.07
#48
#32
#17
#1
5.8±0.4
Bottom View
0.4±0.1
0.5
0.2±0.05
0.025±0.025
0.75±0.05
(0.85±0.05)

3.4 QFN76


9.0±0.1
#58
Top View
#76
#1
#19
9.0±0.1
0.2±0.05
#57
#38
6.9 +0.3 −1.7
Bottom View
#20
#1
0.4±0.1
0.4
0.2±0.05
0.025±0.025
0.75±0.05
(0.85±0.05)

3.5 QFN88


10.0±0.1
#67
#88
#1
#22
Top View
10.0±0.1
0.2±0.05
#66
#44
#23
#1
5.7 +1.5 −0.2
Bottom View
0.4±0.1
0.4
0.2±0.05
0.025±0.025
0.75±0.05
(0.85±0.05)